WEST

End of Result Set

Generate Collection Print

L3: Entry 1 of 1 File: USPT Oct 1, 2002

DOCUMENT-IDENTIFIER: US 6460148 B2
TITLE: Enhanced embedded logic analyzer

Abstract Text (1):
Embedding a logic analyzer in a programmable logic device allows signals to be captured both before and after a trigger condition (breakpoint). A logic analyzer embedded within a PLD captures and stores logic signals. It unloads these signals for viewing on a computer. Using an electronic design automation (EDA) software tool running on a computer system, an engineer specifies signals of the PLD to be monitored, a breakpoint, total number of samples to be stored, number of samples to be captured after the breakpoint occurs, and a system clock signal. The EDA tool automatically inserts the logic analyzer into the electronic design of the PLD which is compiled and downloaded to configure the PLD. Using an interface connected between the PLD and the computer, the EDA tool commands the embedded logic analyzer to run. Signals are stored continuously while running in a ring buffer RAM memory. Once the breakpoint occurs, more samples are captured if desired, in addition to those signals captured before breakpoint. The EDA tool directs the logic analyzer to unload the data from its capture buffer for display on a computer. The breakpoint and sample number can be changed without recompiling. A JTAG port controls the logic analyzer. Inputs and outputs of the logic analyzer are routed to unbonded JTAG-enabled I/O cells. Alternatively, a user-implemented test data register provides a JTAG-like chain of logic elements through which control and output information is shifted. Stimulus cells provide control information to the logic analyzer, and sense cells retrieve data from the logic analyzer.

US Patent No. (1):
6460148

Brief Summary Text (28):
In one embodiment of the invention, using an electronic design automation (EDA) software tool running on a computer system, an engineer specifies signals of the PLD to be monitored, specifies the number of samples to be captured, specifies a system clock signal, and specifies not only a breakpoint, but also the number of samples needed prior to the breakpoint. (Alternatively, total samples could be specified and/or samples needed after a breakpoint.) The EDA tool then automatically inserts the logic analyzer circuit into the electronic design of the PLD which is compiled and downloaded to configure the PLD. Using an interface connected between the PLD and the computer, the EDA tool communicates with the embedded logic analyzer in order to instruct the logic analyzer to run and to begin capturing data. Once a breakpoint occurs, the logic analyzer determines if more samples need to be captured after the breakpoint. The EDA tool then directs the logic analyzer to unload the data from sample memory and then displays the data on the computer. The logic analyzer circuit may then run again to capture another sequence of sample values.

Detailed Description Text (32):
In step 112, a system clock signal is specified for use by the logic analyzer. Any of a variety of signals available within the device may be specified as a system clock signal. A device clock signal that is relevant to the signals being monitored will typically be chosen as a system clock signal. A multiple of a device clock signal may also be chosen in order to sample signals more frequently.

Detailed Description Text (47):
In step 208 the gate level representation of the logic analyzer circuit from step 206 is connected to the flattened representation of the user design of step 204. This step

makes the logic connections from the inputs of the logic analyzer (breakpoint signals, system clock, signals to monitor) to lines providing the actual signals specified in the user's design. As those signals have previously been specified in steps 108 through 115, the EDA tool is able to find the particular signal lines within its database representation of the electronic design and to make the appropriate connection to an input of the logic analyzer.

Detailed Description Text (52):
Logical connections 262 allow signals from user logic 256 to be transmitted to logic analyzer 260. These signals may include a system clock, trigger signals, signals to monitor, etc. Pins of PLD 16 are used to connect interface signals 264 from the logic analyzer to corresponding connections 266 in electronic system 252. Cable 28 is used to connect these interface signals to computer 18. Alternatively, computer 18 may be directly connected to PLD 16 to transmit interface signals 264 to the PLD. In this manner, computer 18 transmits commands and other information to embedded logic analyzer 260, and receives information from the logic analyzer without directly interrupting or affecting the functional operation of electronic system 252. PLD 16 is thus configured to perform both the functions of user logic 256 and embedded logic analyzer 260.

Detailed Description Text (58):
Signal NextReq 284 is received from computer system 18 and allows retrieval of stored sample data a sample at a time, and indicates that the next sample should be uploaded to computer system 18. Signal StopReq 285 is received from computer system 18 and directs the logic analyzer to enter its stop state and to stop capturing signal samples. Signal RunReq 286 is received from computer system 18 and directs the logic analyzer to begin running and capturing sample data. Signal DoneDump 287 directs the logic analyzer to discontinue dumping data from its memory to the computer system and to enter a stop state. This signal may be received from within the logic analyzer or from the user. Signal Clock 288 is the system clock signal specified in step 112. Signal Clear 289 is a reset signal that clears control state machine 302, sample memory 324 and counter 314.

Detailed Description Text (80):
FIG. 11 illustrates a first embodiment by which JTAG port 272 controls embedded logic analyzer 260 of PLD 16 using groups of unbonded I/O cells 504 and 506. Logic analyzer 260 is embedded in core 502 of PLD 16 and has a system clock 288. Cells 504 deliver signals 514 to the logic analyzer, and cells 506 receive signals 516 from the logic analyzer. Signals 275 represent signals from JTAG port 272 to and from I/O cells 504 and 506. Included are: signal TDI that connects to serial data in (SDI) of the first input cell 504; TDO that connects to serial data out (SDO) of the last output cell 506; and control signals such as Shift 680, Clock 682, Update 684, and Mode 686 that are provided to each cell as required. In this embodiment, JTAG-enabled I/O cells 504 are used to control logic analyzer 260 via input signals 514. Output data and status information signals 516 from logic analyzer 260 is connected to JTAG-enabled I/O cells 506.